AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A ~~one-transistor dynamic random access~~ memory ~~(1T DRAM)~~ device, comprising:

a body region insulated from a substrate;

an insulating layer on a surface of said body region; and

a gate structure on said insulating layer and conformally surrounding a portion of said body region, wherein a width of said body region is sufficient to provide a not fully depleted region.

2. (Currently Amended) The ~~1T DRAM~~ memory device as recited in Claim 1, wherein said width of said body region is greater than a length of said gate structure.

3. (Currently Amended) The ~~1T DRAM~~ memory device as recited in Claim 2, wherein said gate structure is a tri-gate and a ratio of said width of said body region to said gate length is at least about 1.5:1.

4. (Currently Amended) The ~~1T DRAM~~ memory device as recited in Claim 2, wherein said gate structure is a fin-fet and a ratio of said width of said body region to said gate length is at least about 1:1.

5. (Currently Amended) The ~~1T DRAM~~ memory device as recited in Claim 1, wherein said body region is insulated from said substrate by an oxide layer.

6. (Currently Amended) The ~~1T DRAM~~ memory device as recited in Claim 1, wherein said body region is insulated from the substrate by a buried layer of a silicon-on-insulator (SOI) substrate.

7. (Currently Amended) A method of manufacturing a ~~one-transistor dynamic random access~~ memory ~~(1T DRAM)~~ device, comprising:

forming a body region insulated from a substrate;

depositing an insulating layer on a surface of said body region; and

forming a gate structure on said insulating layer and conformally surrounding a portion of said body region, wherein a width of said body region is sufficient to provide a not fully depleted region.

8. (Original) The method as recited in Claim 7, wherein said width of said body region is greater than a length of said gate structure.

9. (Original) The method as recited in Claim 8, wherein said gate length is less than about 35 nanometers.

10. (Original) The method as recited in Claim 7, wherein said body region is formed from a silicon layer of a silicon-on-insulator (SOI) substrate.

11. (Original) The method as recited in Claim 10, wherein forming said body region includes forming a mask by depositing and patterning a resist over said silicon layer and performing an anisotropic etch to remove portions of said silicon layer not protected by said mask.

12. (Original) The method as recited in Claim 11, wherein said mask is a sidewall structure.

13. (Original) The method as recited in Claim 7, wherein said gate structure is a tri-gate.

14. (Original) The method as recited in Claim 13, wherein a ratio of said width of said body region to said gate length is at least about 1.5:1.

15. (Original) The method as recited in Claim 7, wherein said gate structure is a FIN-FET.

16. (Original) The method as recited in Claim 15, a ratio of said width of said body region to said gate length is at least about 1:1.

17. (Original) An integrated circuit, comprising:

a one-transistor dynamic random access memory (1T DRAM) device, including:

a body region insulated from a substrate;

an insulating layer on a surface of said body region; and

a gate structure on said insulating layer and conformally surrounding portions of said body region wherein a width of said body region is sufficient to provide a not fully depleted region;

a logic transistor located on said substrate; and

interconnects to interconnect said 1T DRAM and said logic transistor to form an operative integrated circuit.

18. (Original) The integrated circuit as recited in Claim 17, wherein said logic transistor is a multigate transistor having a logic body region, a width of said logic body region being less than said body width of said 1T DRAM device.

19. (Original) The integrated circuit as recited in Claim 17, wherein said logic transistor further comprises:

a logic body region; and

an insulating layer on said surface of said logic body region, wherein said gate structure is on said insulating layer and said gate structure conformally surrounds portions of said logic body region and said gate length is substantially equal to a height and to a width of said logic body region.

20. (Original) The integrated circuit as recited in Claim 17, wherein a logic body region of said logic transistor is fully depleted.